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Low-Complexity Pipelined Architecture For Fbmc/Oqam Transmitter

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ABSTRACT : *In this paper we propose cyclic prefix less Filter-Bank Multi-Carrier with Offset Quadrature Amplitude Modulation (FBMC/OQAM) system over OFDM for next generation wireless standards. We proved that overall throughput metrics of OFDM system in fact largely limits by delay insertion and also depends on many parameters and even with multistage pipelining data rate can't be extended up to 5G requirements. Therefore, the availability of efficient hardware implementations with maximum operating frequency becomes of high interest. In this work, pipelined hardware with maximized parallel processing architecture is used at the transmitter which capable of supporting several filter lengths with low complexity and its efficiency is compared with OFDM implementations. For a functional verification extensive test bench simulation is carry out and proposed architecture complexity analyzes in terms of multipliers used and memory resources with respect to a typical OFDM transmitter. Finally through hardware synthesis, its complexity gap and high throughput to OFDM is proved in implementation perspectives.*

I. Introduction

In telecommunications, 4G is the fourth generation of cellular wireless standards. It is a successor to 3G and 2G families of standards. Multi-band orthogonal frequency-division multiplexing (MB-OFDM) is one of 4G ultra wideband (UWB) radio standards, which provides high-speed connectivity in a wireless personal area network (PAN) [1] with specification of the data rates from 53.3 to 480 Mbps [2]. Due to the high data rates, the MB-OFDM standard requires to process large amount of computations in very short time; its modem has to compute one symbol that consists of 165 complex numbers in every 312.5 ns. Even though its performance requirement results in large hardware complexity, a low power design with small chip size is absolutely essential for applying this technology to portable handheld devices. Also, an operating frequency of a circuit is one of the dominant factors that determine power consumption.

In MB-OFDM, the standard specification defines a sampling frequency of 528 MHz Such high frequency is problematic when we use it as a system clock speed; it consumes too much power and it is hard to implement due to timing constraints. Therefore, parallel architectures have been proposed in an effort to reduce power consumption as well as to relax timing constraints. Exploiting parallelism with 4-way parallel architecture enables to keep throughput constraint at time, lower clock speed.

Despite of the increased hardware resources, it is possible to reduce power consumption as well as to relax timing constraints due to two reasons. First, X way parallel architecture compensates for X times longer gate delays. Therefore, the parallel hardware can operate at reduced supply voltages and consequently consume less power. However, supply voltage scaling is beyond this paper's scope: our work focused on high level resource optimization. Second, a resource efficient design, on which this paper focuses, is able to avoid the linear i.e., times, resource increments.

II. Existing System

In OFDM, information bits to be transmitted are first modulated to generate complex In-phase I and Quadrature Q components cn(m). A maximum of M QAM symbols are modulated, corresponding to the number of active sub-carriers of OFDM.

Then, an IFFT of length M (IFFTM) is computed and a block of M complex samples is generated in time domain. Unused sub-carriers are padded to zero at the input of the IFFT. The baseband OFDM modulation in discrete time domain

III. Proposed System

For the sake of simplicity, a MB-OFDM system consisting only three bands is described here in. Figure 1 illustrates how the OFDM symbols are transmitted in a MB-OFDM system. In this example, it has been

implicitly assumed that the time-frequency coding (TFC) is performed across just three OFDM symbols; however, in practice, the TFC pattern can have a much longer periodicity.

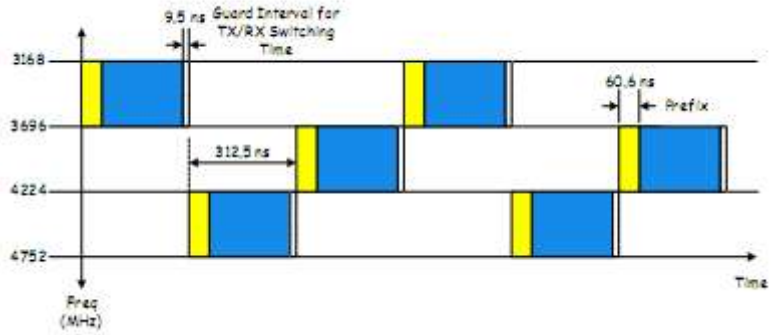

Figure 3.1: coding for an MB-OFDM system

In a MB-OFDM system, a guard interval (9.5 nanoseconds) is appended to each OFDM symbol and a zero-padded prefix (60.6 nanoseconds) is inserted at the beginning of each OFDM symbol. The guard interval ensures that there is sufficient time for the transmitter and receiver to switch to the next carrier frequency.

The structure of the MB-OFDM solution is very similar to that of a conventional wireless OFDM physical layer, except that the carrier frequency is changed based on the time-frequency code. In addition, other modifications have been made to reduce the area and size.

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IV. Architecture Diagram

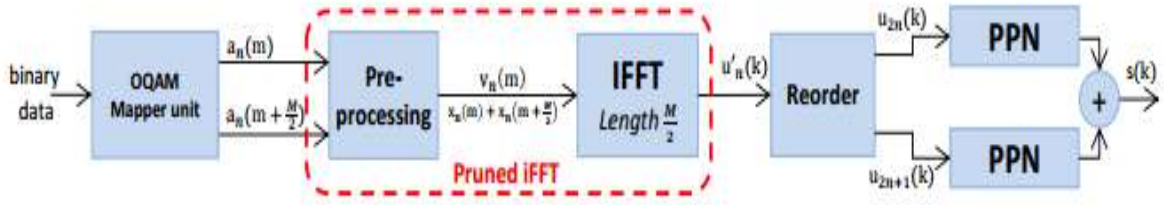

FIG : Optimized FBMC/OQAM hardware architecture using pruned IFFT algorithm

V. Conclusion

Offset modulation combined FMBC pipelined FFT architecture has been proposed for OFDM-based WPAN applications. Highly parallelized FBMC/OQAM transmitter is designed and its complexity and performance gap over OFDM is well proved using FPGA synthesis. Analytical FPGA synthesis results of the proposed cyclic prefix less FBMC transmitter shows significant throughput enhancement over OFDM methods.

FUTURE ENHANCEMENT

In this paper we carried out FFT with combined FBMC pipelined FFT architecture. To reduce the complexity further multiplier less shift based accumulation will be proposed. In order to reduce overall latency of accumulation prefix based arithmetic computation will be added.

References

[1]. chao-wang huang, pang-an ting, and chia-chi "A Novel Message IC Canceller.". transactions on wireless communications, vol 10, NO.4 2011.
[2]. A. Ghaderipoor and C. Tellambura, "Optimal precoder for rate Proc. IEEE International Conf. Commun., Glasgow, Scotland, June 2007.
[3]. H. Jafarkhani, "A quasi-orthogonal space-time block code, " IEEE Trans. Commun., vol 49, no. 1, pp. 1-4, Jan. 2001.
[4]. J. Kazemitabar and H. Jafarkhani, "Multiuser interference cancellation and detection for users with more than two transmit antennas," IEEE Trans. Commun., vol. 56, Apr. 2008.

[5]. A. F. Naguib, N. Seshadri, and A. R. Calderbank, "Application capacity and high data rate wireless systems," in Proc. 1998.
[6]. A. Scaglione, P. Stoica, S. Barbarossa, G. Giannakis, and H. Sampath, "Optimal designs for linear precoder," IEEE Trans Process., vol. 50, no. 5, pp. - 1902-1905, 2002.
[7]. J. Kazemitabar and H. Jafarkhani, "Performance analysis of mul antenna multi-user detection," in Proc. 2009 Workshop Inf.
[8]. D. Love and R. J. Heath, "Limited feedback unitary precoding for orthogonal space-time block codes," IEEE Trans. Signal Process., vol. 53, no. 1, pp. 64-73, 2005.
[9]. A. Paulraj, "Linear precoding for space-time code and systems with known fading correlations," IEEE Commun.